REMARKS

The Office Action mailed April 25, 2002, has been received and reviewed. Claims 1 through 26 and 72 through 102 are currently pending in the application. Claims 1 through 24, 72 through 74, and 78 through 102 stand rejected. Claim 75 has been objected to on the basis of certain writing informalities. Claims 25, 26, 76 and 77 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. New claims 103 through 106 have been added. Applicant respectfully requests reconsideration of the application in view of the amendments and remarks herein.

Information Disclosure Statement

Applicant notes the filing of an Information Disclosure Statement herein on March 29, 2002 and notes that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

Claim Objections Based Upon Writing Informalities

Claims 1 through 26 and 72 through 102 are objected to because of writing informalities. Applicant has amended the claims as suggested by the Examiner. Specifically, the claims were amended to recite a "metal containing layer" and the claims were amended to recite a "first dielectric layer" where appropriate. Reconsideration and withdrawal of the objection is requested.

35 U.S.C. § 112 Claim Rejections

Claims 81 and 87 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, claims 81 and 87 were rejected for lack of antecedent basis.

Applicant has amended claim 81 to recite "[the] a first metal containing layer of the at least one metal containing layer and the substrate". Claim 87 has been amended to recite "wherein said flanking at least one [edge] surface". Reconsideration and withdrawal of the rejection is requested.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent 6,020,233 to Kim

Claims 1, 3, 5, 7 through 10, 14, 22, 72 through 74, 79, 80, 83 through 87, 92, and 100 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kim (U.S. Patent 6,020,233). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kim discloses an improved ferroelectric capacitor including an insulating film 205 having a polysilicon diffusion film 210, diffusion barrier (or metal barrier) film 220, lower electrode film 230, ferroelectrode film 250 and upper electrode 260. Spacers 240 may be formed extending from the insulating layer 205 to the Pt lower electrode film 230. (Kim, figures 2, 3B, 3C, 4B; col. 5, lines 1-4).

By way of contrast with Kim, independent claims 1 and 72 of the presently claimed invention recite the similar element of "forming metal spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure". Support for the amendment can be found in the Specification, for example, Figs. 3a, 3b, 5, 6, 7a, 7b, 8a and 9. Instead, Kim discloses spacers 240 extending only from the insulating layer 205 to the Pt lower electrode film 230. (Kim, figures 2, 3B, 3C, 4B; col. 5, lines 1-4). As Kim fails to teach, either expressly or inherently, every element of independent claims 1 and 72 of the presently claimed invention, these claims are not anticipated. Accordingly, independent claims 1 and 72 of the presently claimed invention are allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 9 is further allowable as Kim fails to disclose, either inherently or expressly, forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62).

Claim 10 is further allowable as Kim fails to disclose, either inherently or expressly, forming the metal spacers of titanium or titanium nitride. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62).

Claim 14 is further allowable as Kim fails to disclose, either inherently or expressly, forming the at least one metal containing layer and the metal spacers of a same metal. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62). By contrast, layer 210 is a polysilicon film and layer 220 is preferably TiO_2. (Kim, col. 4, line 33).

Claim 22 is further allowable as Kim fails to disclose, either inherently or expressly, forming a metal spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

Claims 73 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claim 85 is further allowable as Kim fails to disclose, either inherently or expressly, forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62).

Claim 86 is further allowable as Kim fails to disclose, either inherently or expressly, forming the metal spacers of titanium or titanium nitride. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62).

Claim 92 is further allowable as Kim fails to disclose, either inherently or expressly, forming the at least one metal containing layer and the metal spacers of a same metal. Instead, Kim discloses that the spacers 240 comprise a conducting metal which "as the most distinctive feature of the present invention, electrically connects the Pt lower electrode 230 to the polysilicon film 210". (Kim, col. 3, lines 60-62). By contrast, layer 210 is a polysilicon film and layer 220 is preferably TiO_2. (Kim, col. 4, line 33).

Claim 100 is further allowable as Kim fails to disclose, either inherently or expressly, forming a metal spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,020,233 to Kim

Claims 2, 4, 6, 15 through 21, 23, 24, 78, 81, 82, 93 through 99, 101, and 102 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Patent No. 6,020,233). Applicant respectfully traverses this rejection, as hereinafter set forth.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 2, 4, 6, 15 through 21, 23, 24, 78, 81, 82, 93 through 99, 101, and 102 obvious, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al.

Claims 1, 11 through 13, 72 through 74, and 88 through 91 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745). Applicant respectfully traverses this rejection, as hereinafter set forth.

Liu discloses a passivation method of post copper dry etching. Liu discloses a sandwich structure consisting of a bottom barrier layer 4, a copper layer 6 and a top barrier metal layer 8. After formation of this sandwich structure and patterning, the exposed sidewalls are passivated by means of a barrier metal spacer process. Liu teaches that the fully encapsulated copper lines are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines. (Liu, Abstract).

By way of contrast with Liu, claim 1 of the presently claimed invention recites a method for making a metallization structure for a semiconductor device, comprising forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing layer over the first dielectric layer; forming a single conducting layer over the at least one metal containing layer; forming a second dielectric layer over the conducting layer; removing aligned portions of the second dielectric layer, conducting layer, and at least one metal containing layer to form a multilayer structure; and forming metal spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure.

Applicant respectfully submits that Liu fails to teach or suggest every element of the presently claimed invention. Instead, Liu discloses a lower barrier metal layer 4, copper conducting layer 6, an overlying barrier metal layer 8 and a hard mask layer 16. Applicant respectfully disagrees with the examiner's statement that the barrier metal layer 8 of Liu comprises a conducting layer. (Compare, Paper No. 7, page 6 and Liu, col. 3, lines 30-41). Liu teaches the metal barrier layer 8 comprises materials such as TaN, TiN or Ta which are not conducting metals. (Liu, col. 3, lines 39-41). Thus, metal barrier layer 8 is **not** a conducting layer. Regardless, if this statement is accurate, Liu fails to expressly or inherently disclose a single conducting layer as recited in claim 1 because Liu would include a conducting layer 6 and the metal barrier layer 8. Further, Liu does not disclose

forming a second dielectric layer over the conducting layer, but rather discloses forming the hard mask 16 over the second metal barrier layer 8.

Accordingly, Liu fails to teach or suggest every element of independent claim 1. As such, claim 1 is allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 11 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Independent claim 72 of the presently claimed invention is allowable for substantially the same reasons as independent claim 1.

Claims 73 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claim 73 is further allowable as Liu fails to teach or suggest forming a second dielectric layer over said conducting layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Claim 89 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Objections to Claims 25, 26, 76, and 77/Allowable Subject Matter

Applicant notes with appreciation the notice that claims 25, 26, 76, and 77 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form. Applicant submits that independent claims 1 and 72 from which claims 25, 26, 76, and 77 depend are allowable in view of

the amendments and remarks herein. Further, applicant has added new claims 103 through 106. Claims 103 and 105 are claims 25 and 76 placed in independent form. Claims 104 and 106 include the same elements as claims 26 and 77.

CONCLUSION

Claims 1 through 26 and 72 through 106 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

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KWP/ps:dlm
Date: July 11, 2002
Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended twice) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing layer over the first dielectric layer;

forming a single conducting layer over the at least one metal containing layer;

forming a second dielectric layer over the single conducting layer;

removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure; and

forming metal spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure.

3. (Amended twice) The method of claim 2, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereo6f, including TaN or TiN.

4. (Amended three times) The method of claim 3, further comprising forming a second metal containing layer between a first metal containing layer of said at least one metal containing layer and the substrate, said second metal containing layer comprising TiN, TiW, WN, or TaN.

5. (Amended twice) The method of claim 1, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of titanium or titanium nitride.

6. (Amended) The method of claim 1, wherein the at least one metal containing layer is a single metal containing layer and further comprising forming the single metal containing layer of titanium or titanium nitride.

7. (Amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer from at least one of aluminum and copper.

8. (Amended twice) The method of claim 7, wherein said forming the single conducting layer comprises forming the single conducting layer of an aluminum-copper alloy.

11. (Amended twice) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal spacers to extend along the sidewalls of the second dielectric layer.

14. (Amended) The method of claim 1, further comprising forming the at least one metal containing layer and the metal spacers of [the] a same metal.

15. (Amended twice) The method of claim 1, wherein said forming the at least one metal layer containing comprises forming the at least one metal containing layer by vapor deposition.

16. (Amended three times) The method of claim 1, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer by CVD, PVD or PECVD.

17. (Amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

21. (Amended twice) The method of claim 1, wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form

the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing layer.

25. (Amended) The method of claim 1, further comprising[:] removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

72. (Amended) A method for constructing a metallization structure for a semiconductor device, comprising:
providing a substrate having a first dielectric layer underlying at least one metal containing layer;
creating a single conducting layer over the at least one metal containing layer;
removing aligned portions of the single conducting layer and at least one metal containing layer to form a multilayer structure; and
flanking at least one surface of the multilayer structure with a metal spacer, said metal spacer being substantially the same height as said multilayer structure.

73. (Amended) The method of claim 72, further comprising forming a second dielectric layer over said single conducting layer.

78. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

79. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing layer comprises forming the at least one metal containing layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (Amended) The method of claim 79, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of titanium or titanium nitride.

81. (Amended) The method of claim 72, further comprising forming a second metal containing layer between [the] a first metal containing layer of the at least one metal containing layer and the substrate, said second metal containing layer comprising TiN, TiW, WN, or TaN.

82. (Amended) The method of claim 72, wherein the at least one metal containing layer is a single metal containing layer and further comprising forming the single metal containing layer of titanium or titanium nitride.

83. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises forming the single conducting layer from at least one of aluminum and copper.

84. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises creating the single conducting layer of an aluminum-copper alloy.

87. (Amended) The method of claim 72, wherein said flanking at least one [edge] surface comprises forming said metal spacer on sidewalls of said multilayer structure.

89. (Amended) The method of claim 72, further comprising forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal spacer to extend along the sidewalls of the second dielectric layer.

92. (Amended) The method of claim 72, further comprising forming the at least one metal containing layer and the metal spacer of [the] a same metal.

93. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing layer comprises forming the at least one metal containing layer by vapor deposition.

94. (Amended) The method of claim 93, wherein said forming the at least one metal containing layer by vapor deposition comprises forming the at least one metal containing layer by CVD, PVD or PECVD.

95. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises forming the conducting layer by vapor deposition.

96. (Amended) The method of claim 95, wherein said forming the single conducting layer by vapor deposition comprises forming the single conducting layer by CVD, PVD or PECVD.

99. (Amended) The method of claim 72, wherein removing aligned portions of the single conducting layer and at least one metal containing layer to form a multilayer structure is effected by patterning and etching the single conducting layer and the at least one metal containing layer.

101. (Amended) The method of claim 100, wherein said forming the metal spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

Please add the following new claims:

103. (New) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing layer over the first dielectric layer;

forming a conducting layer over the at least one metal containing layer;

forming a second dielectric layer over the conducting layer;

removing aligned portions of the second dielectric layer, conducting layer, and at least one metal containing layer to form a multilayer structure;

forming metal spacers on sidewalls of the multilayer structure; and

removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

104. (New) The method of claim 103, wherein said removing any remaining portion is effected by etching.

105. (New) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing layer;

creating a conducting layer over the at least one metal containing layer;

removing aligned portions of the conducting layer and at least one metal containing layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal spacer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal spacer layer laterally adjacent thereto.

106. (New) The method of claim 105, wherein said removing any remaining portion is effected by etching.